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QUY CHUẨN KỸ THUẬT QUỐC GIA VỀ ĐẶC TÍNH ĐIỆN/VẬT LÝ CỦA CÁC GIAO DIỆN ĐIỆN PHÂN CẤP SỐ

National technical regulation on physical/electrical characteristics of hierarchical digital interfaces

(for information only)

HA NOI - 2010

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Foreword

QCVN 02:2010/BTTTT is based on ITU Rec. G.703 (11/2001), G.704 (10/1998).

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QUY CHUẨN KỸ THUẬT QUỐC GIA
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National technical regulation
on physical/electrical characteristics of hierarchical digital interfaces

1. GENERAL

1.1. Scope

This technical regulation defines physical and electrical characteristics of the interfaces at hierarchical bit rates (64 kbit/s, 2048 kbit/s, 34368 kbit/s, 139264 kbit/s, 155520 kbit/s and 2048 kbit/s synchronous interfaces) to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection.

1.2. Objectives

This technical regulation applies to telecommunication companies for establishing and providing services when they are in negotiating for network connecting with others via hierarchical digital interfaces.

1.3. Definitions

Wander, jitter

Short-term phase variations of the received digital signal from their ideal positions.

Wander is phase variations that the frequency is 10 Hz or greater.

Jitter is phase variations that the frequency is lower than 10 Hz.

Input jitter tolerance

Input jitter tolerance of a equipment is maximum amplitude and frequency of a jitter which is allowed for each transmission rate at input interface of the equipment.

Output jitter

Generated jitter by equipment is determined by total of jitters at output of equipment when input signal have no jitter.

Time interval error

Peak-peak variation in delay time of a digital signal in comparing with a ideal timing signal in a observed period.

Maximum time interval error

Maximum peak-peak variation in delay time of a digital signal in comparing with a ideal timing signal in a observed period.

1.4. Abbreviations

AIS	Alarm Indication Signal
CMI	Coded Mark Inversion
CODEC	Coder and Decoder
HDB3	High Density Bipolar of order 3 code
PCM	Pulse Code Modulation

PDH	Plesiochronous Digital Hierarchy
SDH	Synchronous Digital Hierarchy
STM	Synchronous Transport Module
STM-1	Synchronous Transport Module 1
UI	Unit Interval

2. TECHNICAL REQUIREMENTS

2.1. Interface at 64 kbit/s (E0)

2.1.1. Functional requirements

- Nominal bit rate: 64 kbit/s.

- Tolerance: $\pm 10^{-5}$.

Interfaces at 64 kbit/s are including codirectional interface, centralized clock interface and contradirectional interface.

Three signals can be carried across the interface:

- 64 kbit/s information signal;

- 64 kHz timing signal;

- 8 kHz timing signal.

2.1.1.1. Codirectional interface

The term "codirectional" is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (Figure 1).

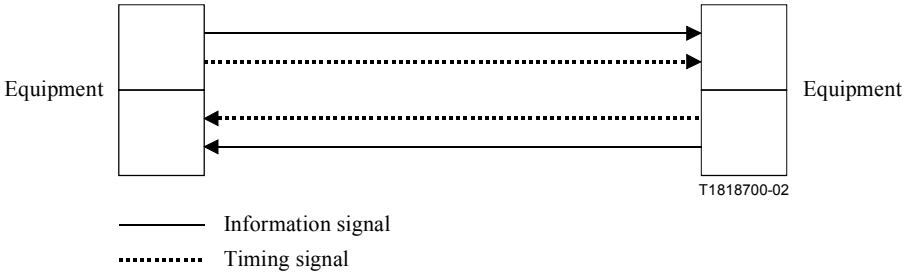


Figure 1 – Codirectional interface

2.1.1.2. Centralized clock interface

The term "centralized clock" is used to describe an interface wherein for both directions of transmission of the information signal, the associated timing signals are supplied from a centralized clock, which may be derived for example from certain incoming line signals (Figure 2).

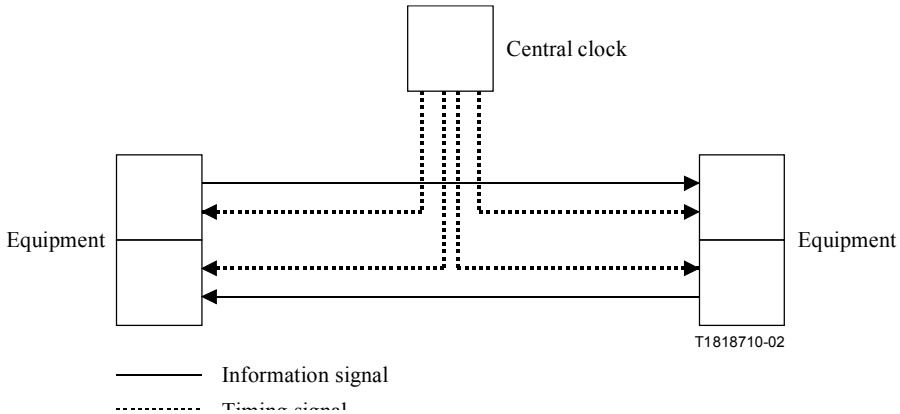


Figure 2 – Centralized clock interface

2.1.1.3. Contradirectional interface

The term "contradirectional" is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (Figure 3).

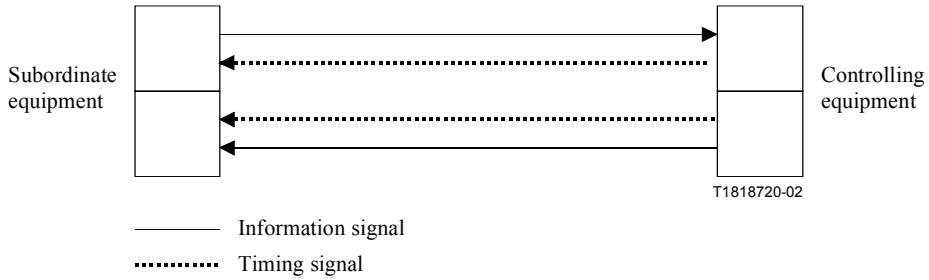


Figure 3 – Contradirectional interface

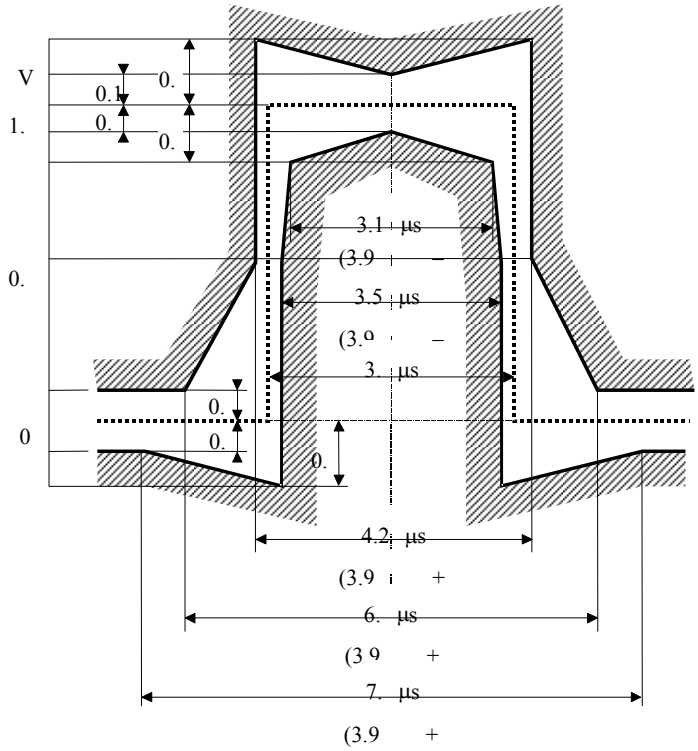
2.1.2. Electrical characteristics of 64 kbit/s codirectional interface

2.1.2.1. Specifications at the output ports

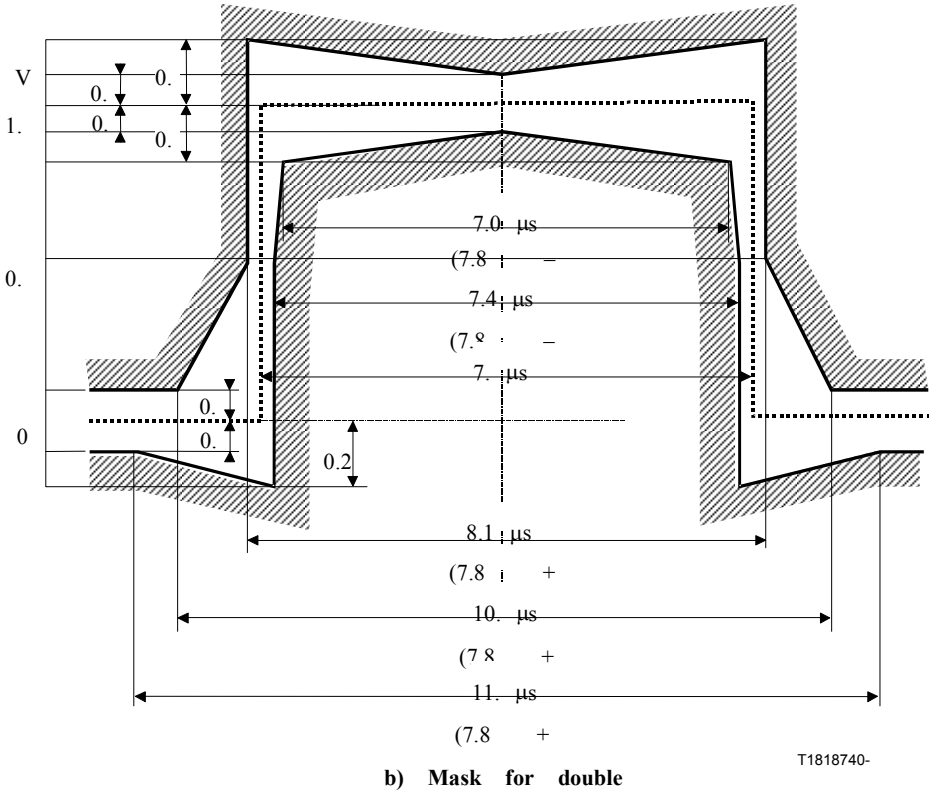
Specifications at the output ports shall be compliance with technical requirements in Figure 4, 5 and Table 1.

Table 1 – Digital 64 kbit/s codirectional interface

Symbol rate	256 kBauds
Pair for each direction	One symmetric pair
Pulse shape	Nominally rectangular
Test load impedance	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.10 V
Nominal pulse width	3.9 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulses interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05



a) Mask for single



b) Mask for double

Figure 4, 5 – Pulse masks of the 64 kbit/s codirectional interface

2.2.2.2. Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 128 kHz should be in the range 0 to 3 dB.

The return loss at the input ports should have the following minimum values in Table 2.

Table 2 – Minimum return loss at the input ports of the 64 kbit/s codirectional interface

Frequency range (kHz)	Return loss (dB)
4 to 13	12
13 to 256	18
256 to 384	14

2.1.3. Electrical characteristics of the 64 kbit/s centralized clock interface

For each direction of transmission, there should be one symmetrical pair carrying the data signal. In addition, there should be symmetrical pairs carrying the composite timing signal (64 kHz and 8 kHz) from the central clock source to the office terminal equipment. The use of transformers is recommended.

The structure of the signals and their nominal phase relationships are shown in Figure 6.

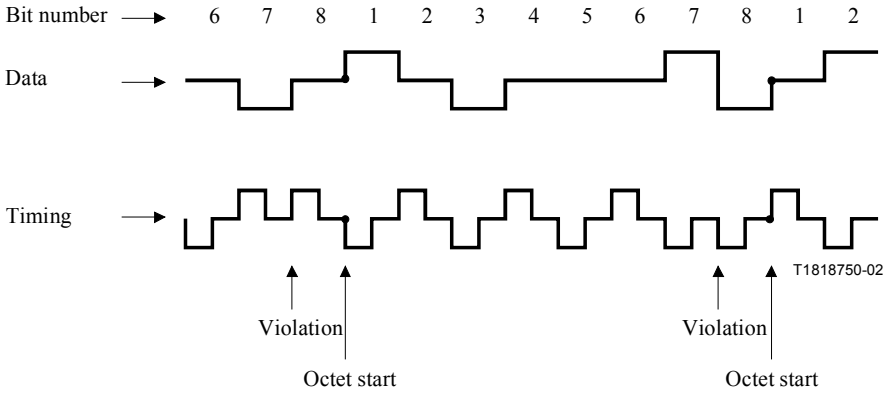


Figure 6 – Signal structures of the 64-kbit/s central clock interface at office terminal output ports

2.1.3.1. Characteristics at the output ports

Characteristics at the output ports of the 64-kbit/s central clock interface are shown in Table 2.

Table 2 – Digital 64 kbit/s centralized clock interface

Parameters	Data	Timing
Pulse shape	Nominally rectangular, with rise and fall times less than 1 μs	Nominally rectangular, with rise and fall times less than 1 μs
Nominal test load impedance	110 ohms resistive	110 ohms resistive
Peak voltage of a "mark" (pulse) (Note 1)	a) 1.0 ± 0.1 V b) 3.4 ± 0.5 V	a) 1.0 ± 0.1 V b) 3.0 ± 0.5 V

Peak value of a "space" (no pulse) (Note 1)	a) 0 ± 0.1 V b) 0 ± 0.5 V	a) 0 ± 0.1 V b) 0 ± 0.5 V
Nominal pulse width (Note 1)	a) 15.6 μs b) 15.6 μs	a) 7.8 μs b) 9.8 to 10.9 μs
Maximum peak-to-peak jitter at the output port (Note 2)	Refer to 5.1/G.823	
NOTE – The choice between the set of parameters a) and b) allows for different office noise environments and different maximum cable lengths between the three involved office equipments.		

2.1.3.2. Characteristics at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs.

The varying parameters in Table 2 will allow typical maximum interconnecting distances of 350 to 450 m.

2.1.4. Electrical characteristics of 64 kbit/s contradirectional interface

The structures of the signals and their phase relationships at data output ports are shown in Figure 7.

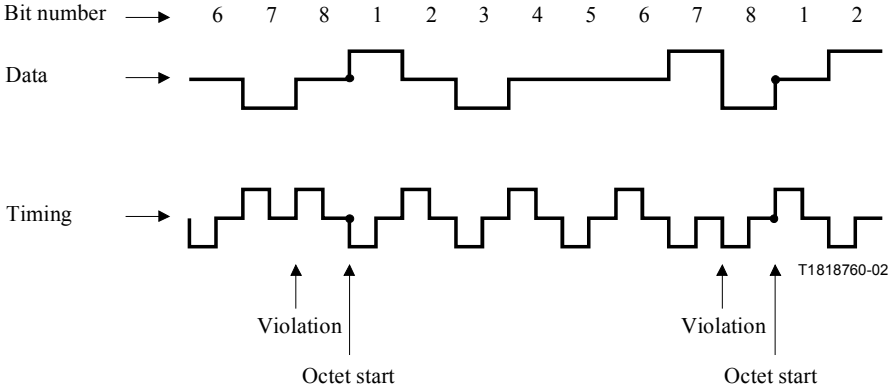


Figure 7 – Signal structures of the 64-kbit/s contradirectional interface at data output ports

2.1.4.1. Specifications at the output ports

Specifications at the output ports of the 64-kbit/s contradirectional interface are shown in Figure 8,9 and Table 3.

Table 3 – Digital 64 kbit/s contradirectional interface

Parameters	Data	Timing
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the mask in Figure 8 irrespective of the polarity	All pulses of a valid signal must conform to the mask in Figure 9 irrespective of the polarity
Pairs in each direction of transmission	One symmetric pair	One symmetric pair
Test load impedance	120 ohms resistive	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V	1.0 V

Peak voltage of a "space" (no pulse)	0 V ± 0.1 V	0 V ± 0.1 V
Nominal pulse width	15.6 μs	7.8 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	0.95 to 1.05

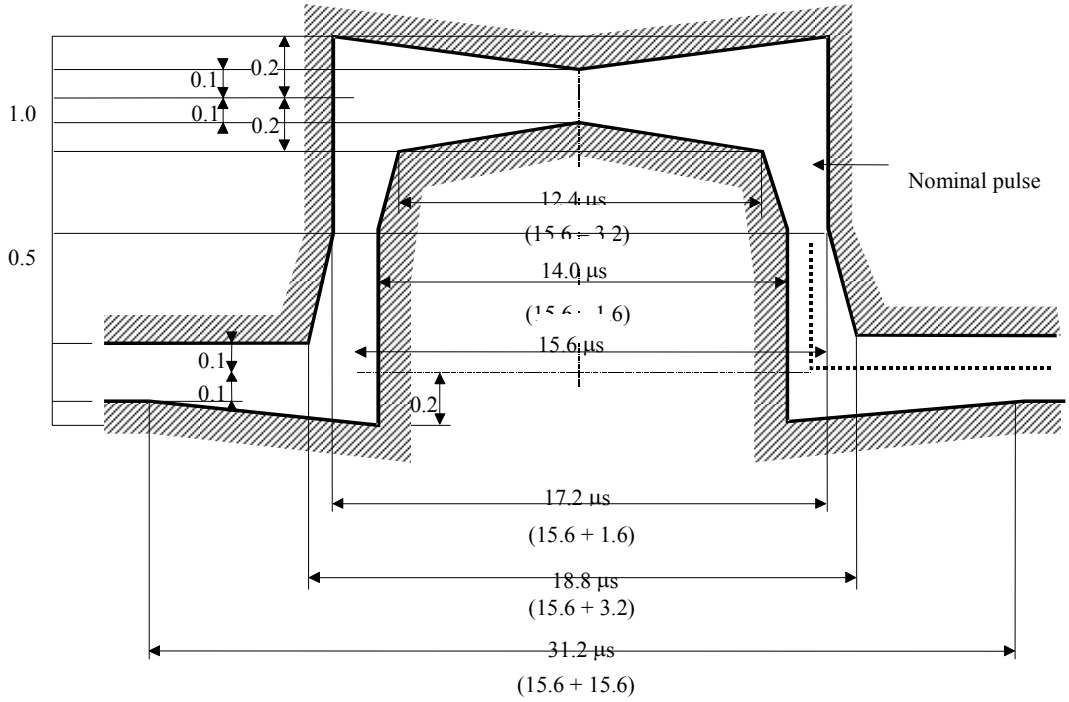


Figure 8 – Mask of the data pulse of the 64-kbit/s contradirectional interface

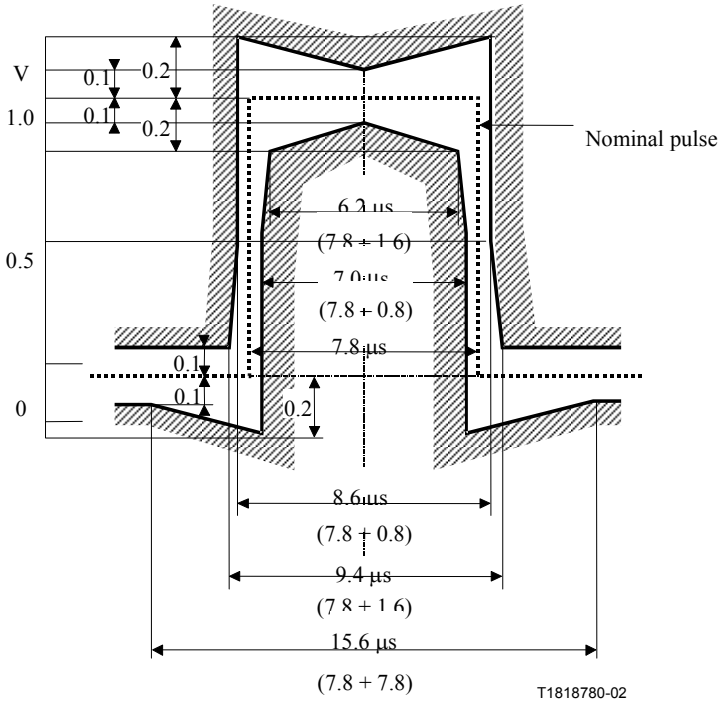


Figure 9 – Mask of the timing pulse of the 64-kbit/s contradirectional interface

2.1.4.2. Specifications at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 32 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The minimum return loss at the input ports should be as in Table 5.

Table 5 - Minimum return loss at the input ports of the 64-kbit/s contradirectional interface

Frequency range (kHz)		Return loss (dB)
Data signal	Composite timing signal	
1.6 to 3.2	3.2 to 6.4	12
3.2 to 64	6.4 to 128	18
64 to 96	128 to 192	14

2.1.5. Overvoltage protection and grounding

Requirements for overvoltage protection: see Annex A.

Requirements for grounding comply with relevan technical regulation on earthing and grouding for telecommunication plants.

2.2. Interface at 2048 kbit/s (E12)

2.2.1. General characteristics

Nominal bit rate: 2048 kbit/s.

Bit rate accuracy: ±50 ppm (±102.4 bit/s).

Code: High density bipolar of order 3 (HDB3).

2.2.2. Specifications at the output ports

Specifications at the output ports of the interface at 2048 kbit/s are shown in Figure 10 and Table 6.

Table 6 – Digital interface at 2048 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 10) irrespective of the sign	
Pair(s) in each direction	One coaxial pair (see 9.4)	One symmetrical pair (see 9.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

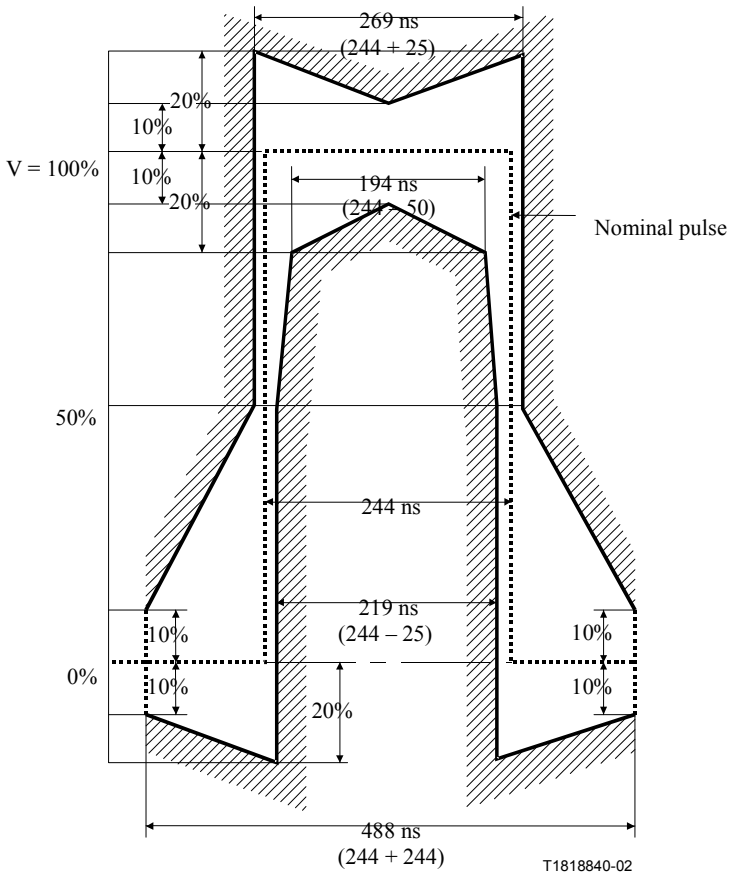


Figure 10 – Mask of the pulse at the 2048 kbit/s interface

2.2.3. Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristic of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. The minimum return loss at the input port should be as in Table 7.

Table 7 - minimum return loss at the input port of the 2048 kbit/s interface

Frequency range (kHz)	Return loss (dB)
51 to 102	12
102 to 2048	18
2048 to 3072	14

2.2.4. Overvoltage protection and grounding

Requirements for overvoltage protection: see Annex A.

Requirements for grounding comply with relevan technical regulation on earthing and grouding for telecommunication plants.

2.2.5. Basic frame structure at 2048 kbit/s

Frame length

256 bits, numbered 1 to 256. The frame repetition rate is 8000 Hz.

Allocation of bits number 1 to 8 of the frame is shown in Table 7B.

Table 7B – Allocation of bits 1 to 8 of the frame

Bit number Alternate frames	1	2	3	4	5	6	7	8
Frame containing the frame alignment signal	S_i	0	0	1	1	0	1	1
	(Note 1)	Frame alignment signal						
Frame not containing the frame alignment signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	(Note 1)	(Note 2)	(Note 3)	(Note 4)				

NOTE 1 – S_i = Bits reserved for international use. If no use is realized, these bits should be fixed at 1 on digital paths crossing an international border.
NOTE 2 – The bit is fixed at 1 to assist in avoiding simulations of the frame alignment signal.
NOTE 3 – A = Remote alarm indication. In undisturbed operation, set to 0; in alarm condition, set to 1.
NOTE 4 – S_{a4} to S_{a8} = Additional spare bits whose use may be as follows:

i) Bits S_{a4} to S_{a8} may be recommended by ITU-T for use in specific point-to-point applications.

ii) Bit S_{a4} may be used as a message-based data link to be recommended by ITU-T for operations, maintenance and performance monitoring. If the data link is accessed at intermediate points with consequent alterations to the S_{a4} bit, the CRC-4 bits must be updated so as to retain the correct end-to-end path termination functions associated with the CRC-4 procedure.

iii) Bits S_{a5} to S_{a7} are for national usage where there is no demand on them for specific point-to-point applications [see i) above].

iv) One of the bits S_{a4} to S_{a8} may be used in a synchronization interface to convey synchronization status messages.

Bits S_{a4} to S_{a8} (where these are not used) should be set to 1 on links crossing an international border.

2.3. Interface at 34 368 kbit/s (E31)

2.3.1. General characteristics

Nominal bit rate: 34 368 kbit/s.

Tolerance: $\pm 10^{-5}$.

Code: HDB3.

2.3.2. Specification at the output ports

Specification at the output ports of the nterface at 34 368 kbit/s shall be as in Figure 11 and Table 8.

Table 8 – Digital interface at 34 368 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 11)
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V $\pm$ 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

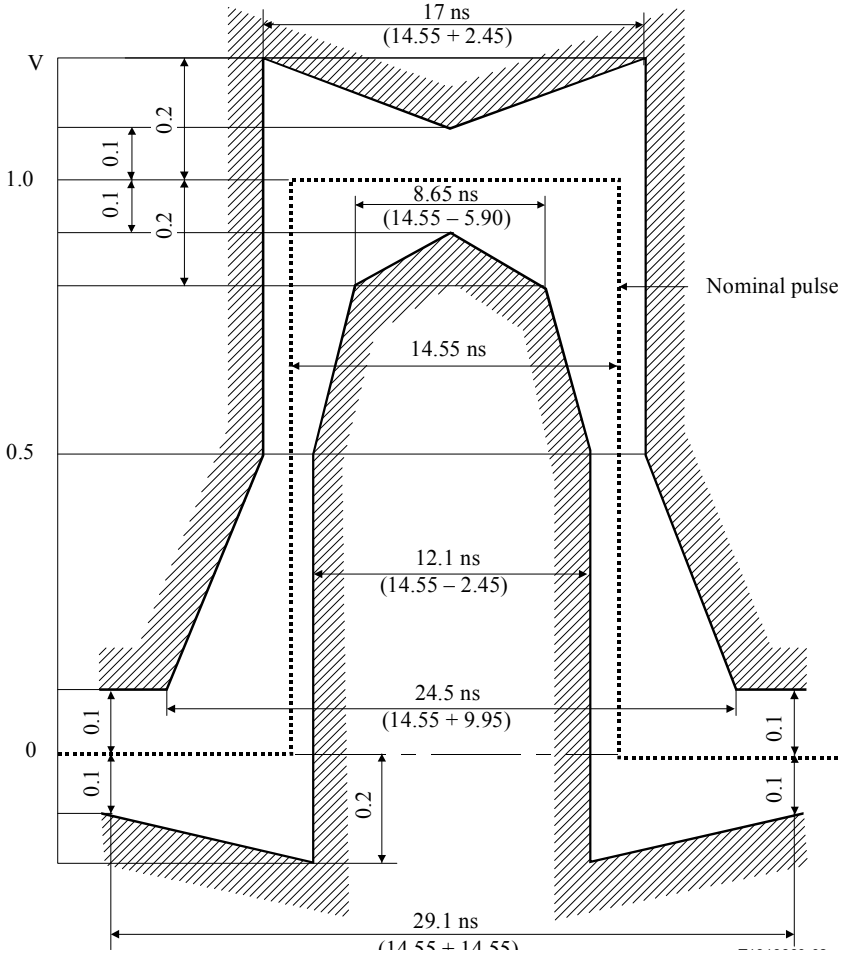


Figure 11 – Pulse mask at the 34 368 kbit/s interface

2.3.3. Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law and the loss at a frequency of 17 184 kHz shall be in the range 0 to 12 dB.

The minimum return loss at the input port Interface at 34 368 kbit/s should be as in Table 9.

Table 9 - Minimum return loss at the input port Interface at 34 368 kbit/s

Frequency range (kHz)	Return loss (dB)
860 to 1720	12
1720 to 34 368	18
34 368 to 51 550	14

2.3.4. Overvoltage protection and grounding

Requirements for overvoltage protection: see Annex A.

Requirements for grounding comply with relevan technical regulation on earthing and grouding for telecommunication plants.

2.3.5. Frame structure at 36368 kbit/s

Basic frame structure at 34 368 kbit/s includes 7 octets of head và 530 octets of payload per each 125 μs as shown in Figure 11B.

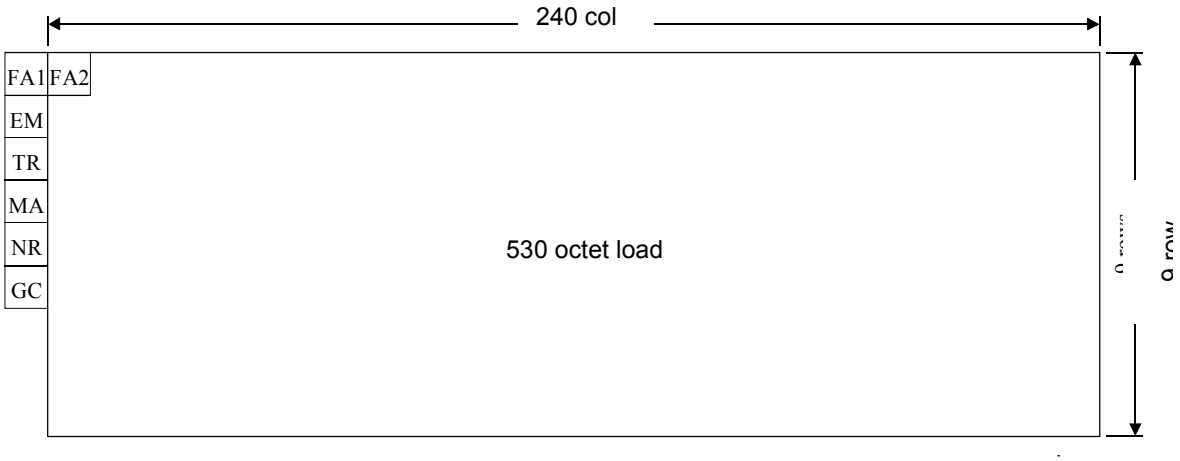


Figure 11B – Frame structure at 34 368 kbit/s

Header distribution

Values and distribution of header bytes is shown in Figure 11C:

FA1	1	1	1	1	0	1	1	0	0	0	1	0	1	0	0	0
EM	BIP-8															
TR	Trail Trace															
MA	RDI	REI	Payload type			MFI		SSM								
NR	NR															
GC	GC															

FA2

Figure 11C – Header distribution at 34 368 kbit/s

FA1/FA2: Frame synchronous signal.

EM: Error management.

BIP-8: One byte is distributed for error management. This function is for a BIP-8 code using even status. BIP-8 is calculated on all the bits, including header bit of previous 125 μs. Caculated BIP-8 is located at the byte EM of existing 125 μs.

TR: This byte is used for repeating traced access point identification (TAPI), so that receiver can check connection-continueing status with intended transmitter.

16 byte frame defined for access point identification

MA adaptive and maintainance byte

Bit 1 RDI

Bit 2 REI – if one or more errors detected by BIP-8, this bit is set by "1" and resent to terminate finding remote trace, others this bit is set by “0”.

Bits 3 to 5 Payload type

Code	Signal
000	Undefined
001	Defined
010	ATM
011	SDH TU-12

Bits 6-7: multiframe indicator

Bit 8: this bit is used in 4-frame multiframe. Status of multiframe is determined by values of bits 6, 7 of MA as following:

Bit 6	Bit 7	Bit 8
0	0	SSM bit 1 (MSB)
0	1	SSM bit 2
1	0	SSM bit 3
1	1	SSM bit 4 (LSB)

Four bits of the multiframe are distributed for synchronous status message (SSM).

NR: This byte is distributed for specific maintainance purposes of each network operators.

GC: General information channel (eg. providing voice/data channel connection for maintainance purposes).

2.4. Interface at 139 264 kbit/s (E4)

2.4.1. General characteristics

Nominal bit rate: 139 264 kbit/s.

Tolerance: $\pm 15.10^{-6}$.

Code: Coded Mark Inversion (CMI).

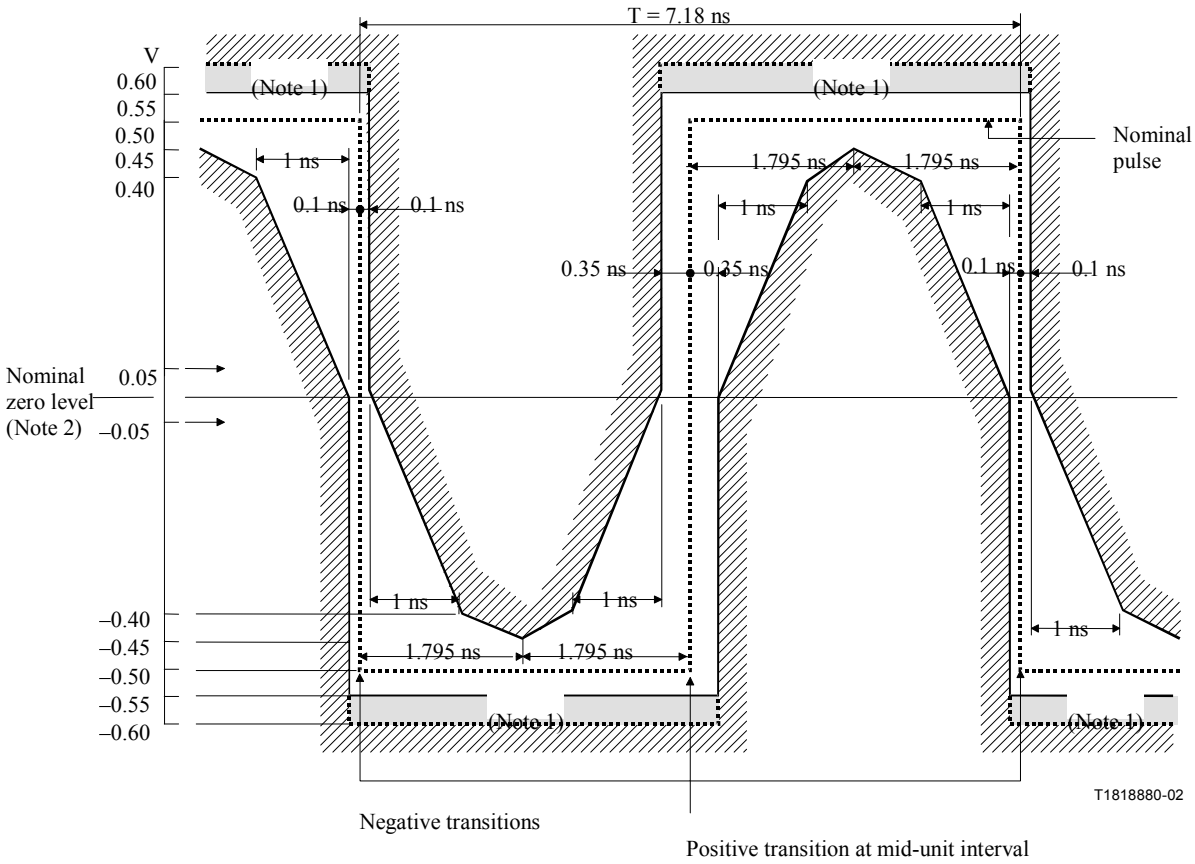
2.4.2. Specifications at the output ports

The specifications at the output ports are given in Table 10 and Figures 12, 13.

Table 10 – Digital interface at 139 264 kbit/s

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 12 and 13
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	$\leq$2 ns

Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transitions)	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-interval: ±0.35 ns
Return loss	≥15 dB over frequency range 7 MHz to 210 MHz

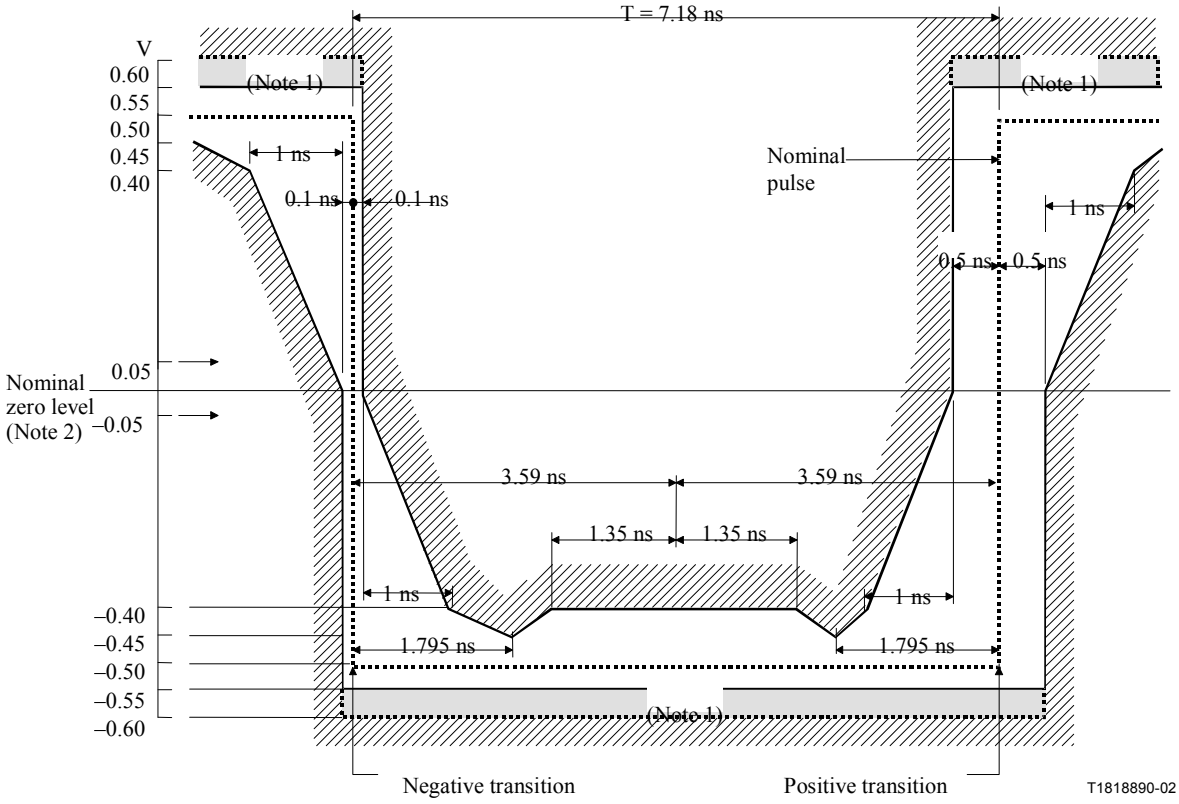


NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

Figure 12 – Mask of a pulse corresponding to a binary 0 at the 139 264 kbit/s interface



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

Figure 13 – Mask of a pulse corresponding to a binary 1 at the 139 264 kbit/s interface

2.4.3. Specifications at the input ports

The digital signal presented at the input port should conform to specification at the input port (Table 10 and Figures 18 and 19), but can be modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

The return loss characteristics should be the same as that specified for the output port.

2.4.4. Overvoltage protection and grounding

Requirements for overvoltage protection: see Annex A.

Requirements for grounding comply with relevan technical regulation on earthing and

grouding for telecommunication plants.

2.4.5. Frame structure at 139264 kbit/s

Basic frame structure at 139264 kbit/s includes 16 octets of header và 2160 octets of payload per each 125 μs as shown in Figure 13B.

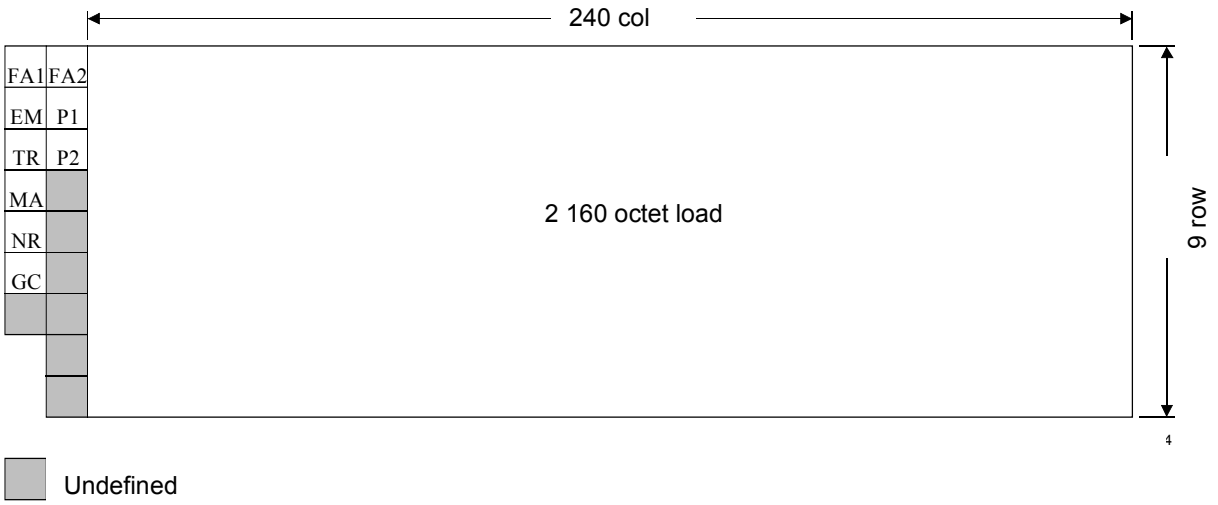


Figure 13B – Frame structure at 139 264 kbit/s

Header distribution

Values and distribution of header bytes is shown in Figure 13C:

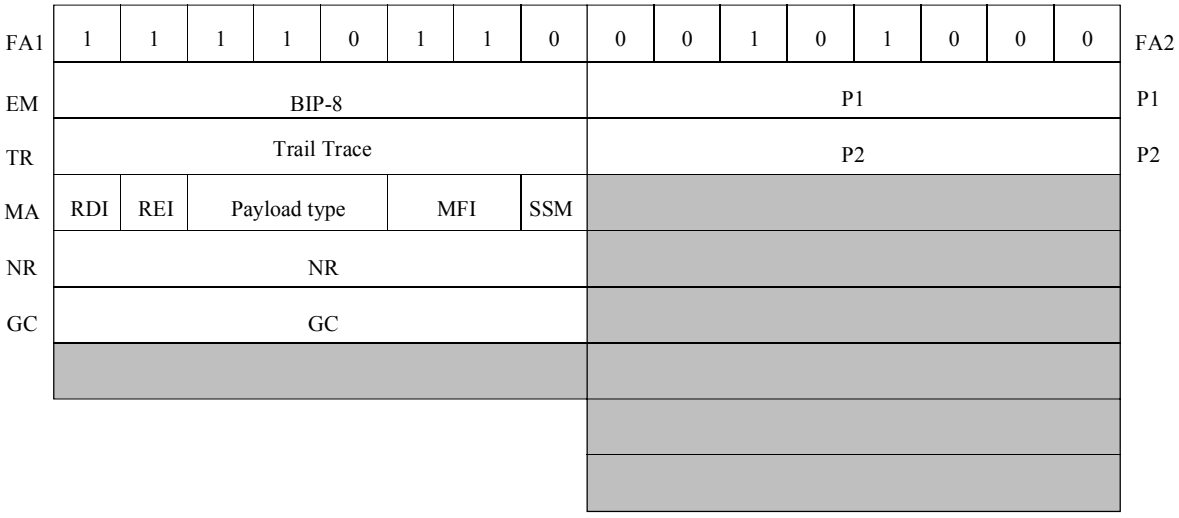


Figure 13C – Header distribution at 139 264 kbit/s

FA1/FA2: Frame synchronous signal.

EM: Error management.

BIP-8: One byte is distributed for error management. This function is for a BIP-8 code using even status. BIP-8 is calculated on all the bits, including header bit of previous 125 μs. Caculated BIP-8 is located at the byte EM of existing 125 μs.

TR: This byte is used for repeating traced access point identification (TAPI), so that receiver can check connection-continueing status with intended transmitter.

16 byte frame defined for access point identification

MA adaptive and maintainance byte

Bit 1 RDI

Bit 2 REI – if one or more errors detected by BIP-8, this bit is set by "1" and resent to terminate finding remote trace, others this bit is set by "0".

Bits 3 to 5 Payload type

Code	Signal	
000	Undefined	
001	Defined	
010	ATM	
011	SDH components type I	20 × TUG-2
100	SDH components type II	2 × TUG-3 and 5 × TUG-2

Bits 6-7 multiframe indication bit

Bit 8 this bit is used in 4-frame multiframe. Status of multiframe is determined by values of bits 6, 7 of MA as following:

Bit 6	Bit 7	Bit 8
0	0	SSM bit 1 (MSB)
0	1	SSM bit 2
1	0	SSM bit 3
1	1	SSM bit 4 (LSB)

Four bits of the multiframe are distributed for synchronous status message (SSM).

NR: This byte is distributed for specific maintainance purposes of each network operators.

GC: General information channel (eg. providing voice/data channel connection for maintainance purposes).

P1/P2

2.5. Interface at 155 520 kbit/s – STM-1 interface (ES1)

2.5.1. General characteristics

Nominal bit rate: 155 520 kbit/s.

Tolerance: $\pm 2.10^{-5}$.

Code: Coded Mark Inversion (CMI).

2.5.2. Specifications at the output ports

The specifications at the output ports are given in Table 11 and in Figure 14, 15.

Table 11 – Digital interface at 155 520 kbit/s

Pulse shape	Nominally rectangular and conforming to the masks shown in Figure 14, 15
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance	Negative transitions: ±0.1 ns (Figure 14, 15) Positive transitions at unit interval boundaries: ±0.5 ns (Figure 15) Positive transitions at mid-unit intervals: ±0.35 ns (Figure 14)
Return loss	≥15 dB over frequency range 8 MHz to 240 MHz

2.5.3. Specifications at the input ports

The digital signal presented at the input port should conform to Table 12 and Figure 15 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12.7 dB at a frequency of 78 MHz.

The return loss characteristics should be the same as that specified for the output port.

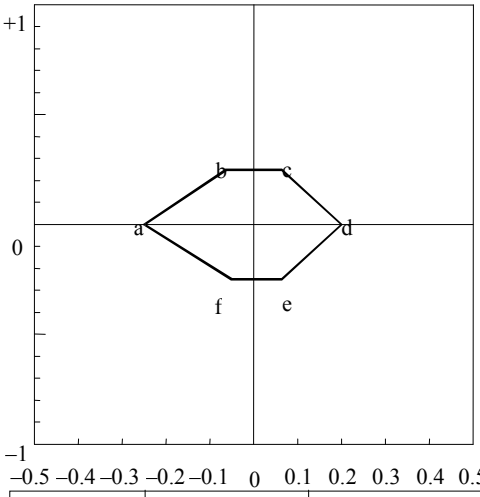
2.5.4. Specifications at the cross-connect points

Signal power level: A wideband power measurement using a power level sensor with a working frequency range of at least 300 MHz shall be between −2.5 and +4.3 dBm. There shall be no DC power transmitted across the interface.

Eye diagram: An eye diagram mask based on the maximum and minimum power levels given above is shown in Figure 16 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the pulse repetition period T. The corner points of the eye diagram are shown in Figure 16.

Termination: One coaxial cable shall be used for each direction of transmission.

Impedance: A resistive test load of 75 ohms ±5% shall be used at the interface for the evaluation of the eye diagram and the electrical parameters of the signal.



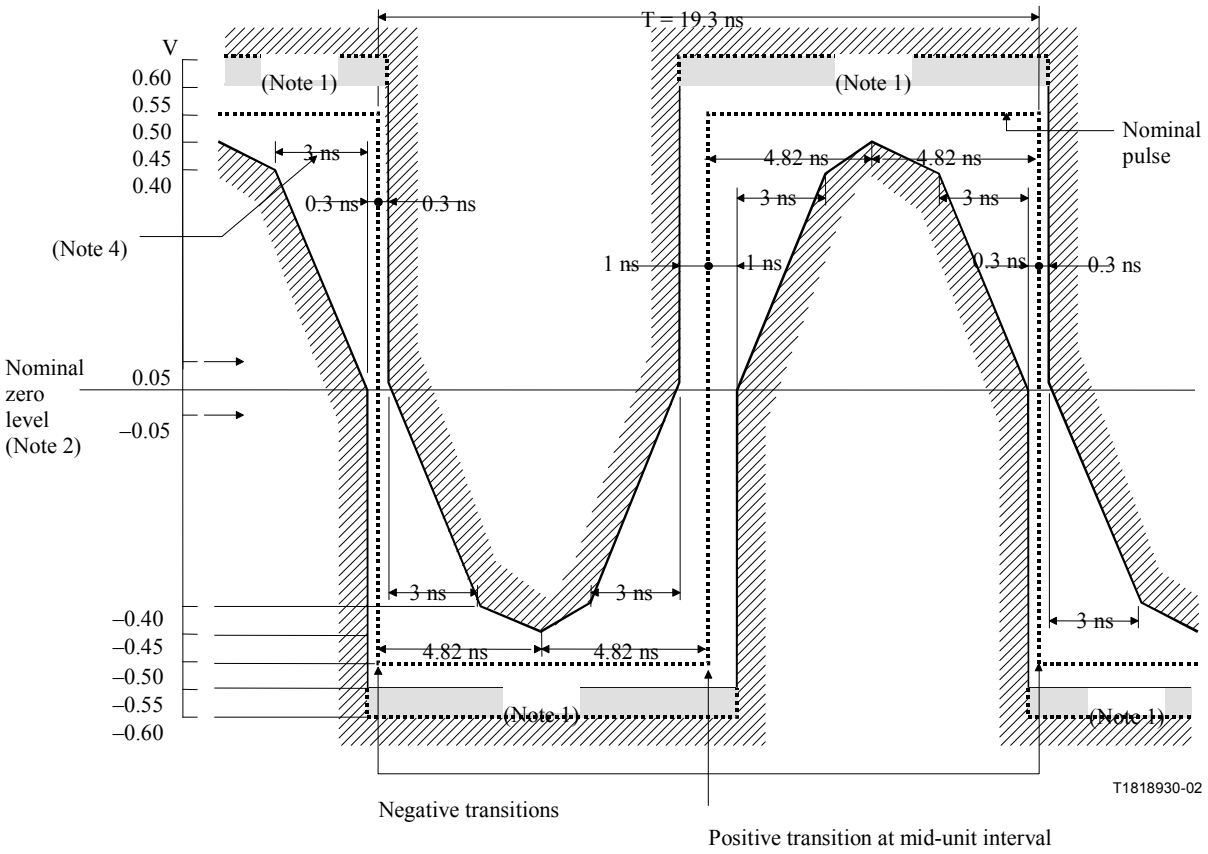
Point	Time	Amplitude
a	$-0.25\frac{T}{2}$	0.00
b	$-0.05\frac{T}{2}$	+0.25
c	$+0.05\frac{T}{2}$	+0.25
d	$+0.20\frac{T}{2}$	0.00
e	$+0.05\frac{T}{2}$	–0.25
f	$-0.05\frac{T}{2}$	–0.25

Figure 16/Table 12 – STM-1 interface eye diagram

2.5.5. Overvoltage protection and grounding

Requirements for overvoltage protection: see Annex A.

Requirements for grounding comply with relevan technical regulation on earthing and grouding for telecommunication plants.



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 Vlimit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal finish and start edges coincident.

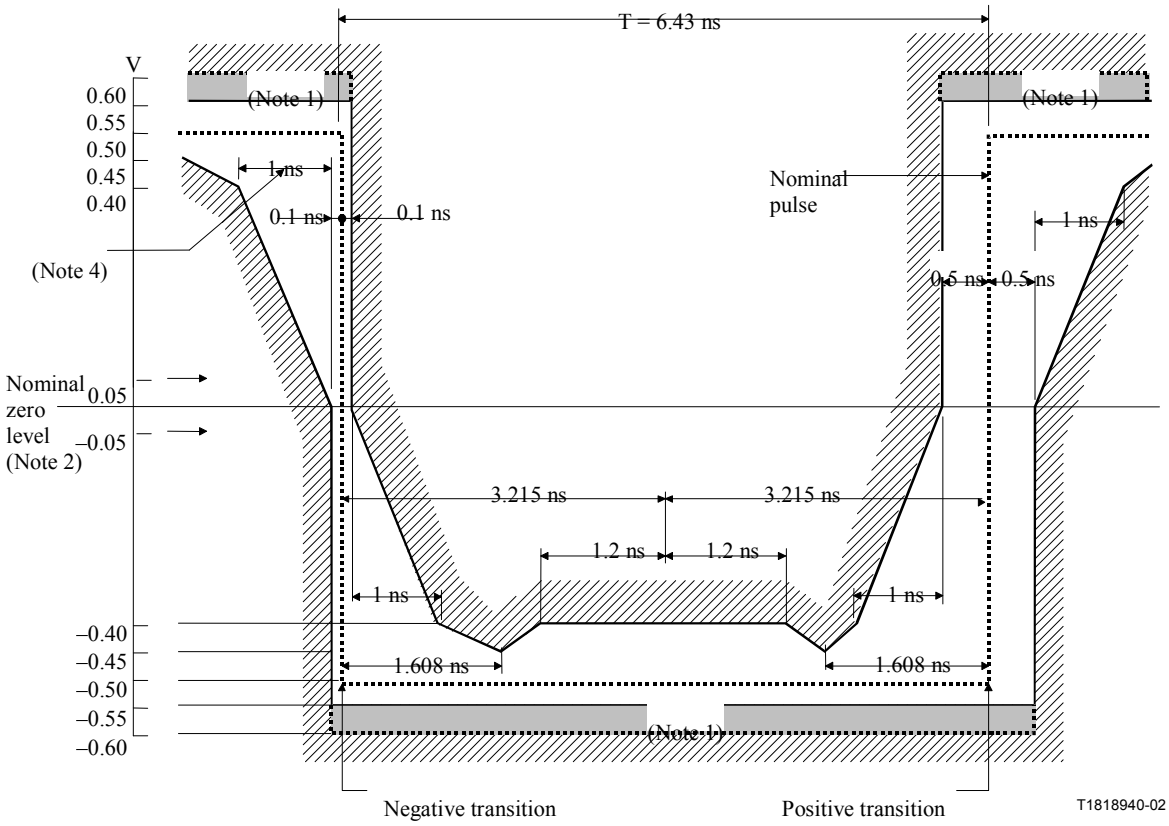
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulse be superimposed in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

Figure 14 – Mask of a pulse corresponding to a binary 0 at the 155 520 kbit/s interface (note 3)



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal starting and finishing edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of pulses be overlayed in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions is ±0.1 ns and ±0.5 ns respectively.

Figure 15 – Mask of a pulse corresponding to a binary 1 at the 155 520 kbit/s interface (notes 3 and 5)

2.6. Synchronization interface at 2048 kHz (T12)

2.6.1. General characteristics

The use of this interface is recommended for all applications where it is required to synchronize a digital equipment by an external 2048 kHz synchronization signal.

2.6.2. Specifications at the output ports

The specifications at the output ports are given in Table 13 and in Figure 17.

Table 13 – Digital 2048 kHz clock interface

Frequency	2048 ± 5.10^{-5} kHz	
Pulse shape	The signal must conform with the mask in Figure 17. The value V corresponds to the maximum peak value. The value V_1 corresponds to the minimum peak value.	
Type of pair	Coaxial pair	Symmetrical pair
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak voltage (V_{op})	1.5	1.9
Minimum peak voltage (V_{op})	0.75	1.0

This value is valid for network timing synchronization equipments.

Other values may be specified for timing output ports of digital links carrying the network timing.

2.6.3. Specifications at the input ports

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 2048 kHz should be in the range 0 to 6 dB (minimum value). The return loss at 2048 kHz should be $\geq$15 dB.

2.6.4. Overvoltage protection and grounding

Requirements for overvoltage protection: see Annex A.

Requirements for grounding comply with relevan technical regulation on earthing and grouding for telecommunication plants.

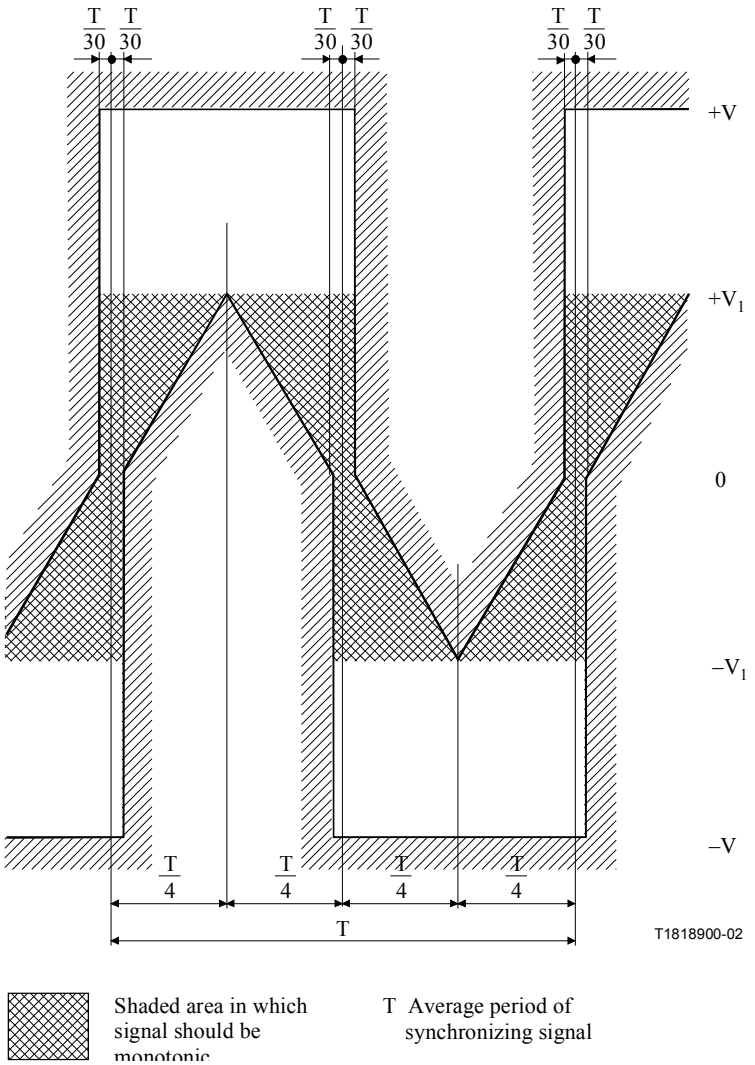


Figure 17 – Wave shape at an output port of the 2048 kHz synchronization interface

3. REGULATION ON MANAGEMENT

3.1. Interfaces in 1.1 must comply with requirements in this technical regulation.

3.2. Interfaces in local networks of telecommunication operatos are encourged to comply with requirements in this technical regulation.

4. RESPONSIBILITY OF ORGANISATIONS/INDIVIDUALS

4.1. Telecommunication operators in Vietnam are responsible to comply with this technical regulation when negotiating for connection with others.

and to accept supervision of regulatory authority as existing regulations.

4.2. This technical regulation shall be the technical basis for resolving disputes.

4.3. If the agreement is included with requirements which are not in this technical rgulation, operators shall be responsible with relating problems.

5. IMPLEMENTATION

5.1. Telecommunication Authorities are responsible to instruct and implement this technical regulation.

5.2. This technical regulation superseded TCN 68-172:1998 and TCN 68-175:1998.

5.2. In cases of referencing regulations changed, modified or superseded, new versions is applied.

ANNEX A
(Normative)
Overvoltage protection requirements

Telecommunication equipments with hierarchical digital interfaces shall comply with relevan technical regulations for overvoltage, overcurrent protection.

Inputs/outputs of hierarchical digital interfaces shall comply with test of 10 standard surges with maximum amplitude U (5 positives and 5 negatives).

A.1. Interfaces using coaxial cable

Use surge generator as in Figure A.1 (voltage diferential modes).

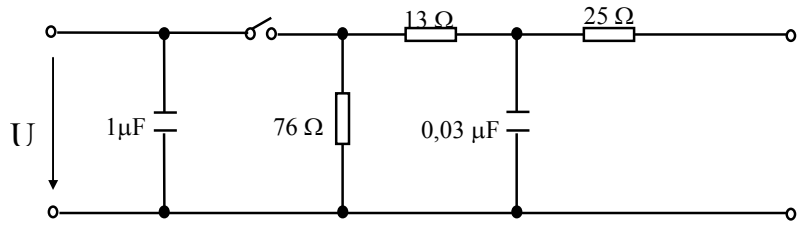


Figure A.1 - 1,2/50 μs surge generator for coaxial cable

A.2. Interfaces using balanced cable

Use surge generator as in Figure A.2 (voltage commmon mode: U = 100 V_{dc})

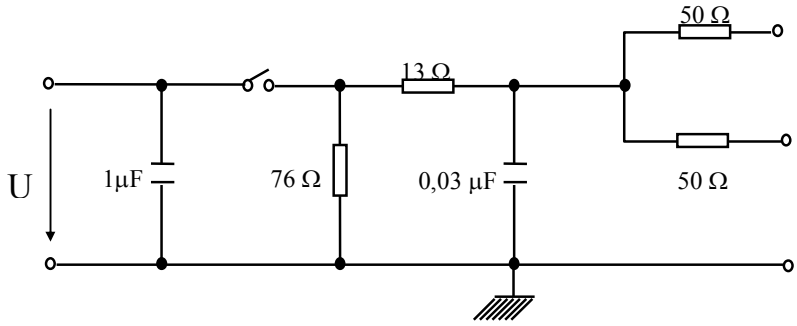


Figure A.2 - 1,2/50 μs surge generator for balanced cable